

What is claimed is:

- 1     1.     A flip flop comprising:  
2             a state retention portion to store a bit of digital data, said state retention portion  
3     having a first storage node and a second storage node; and  
4             a clocking portion to transfer a new bit of digital data to said state retention  
5     portion in response to a clock signal, said clocking portion including:  
6             a first stack of transistors coupled to said first storage node to draw  
7             current from said first storage node when a first digital data value is being  
8             transferred to said state retention portion, said first stack of transistors including  
9             a first transistor having a gate terminal coupled to receive said clock signal and  
10            a second transistor having a gate terminal coupled to receive a delayed, inverted  
11            version of said clock signal.
  
- 1     2.     The flip flop of claim 1, wherein:  
2             said first and second transistors are N-type insulated gate field effect transistors  
3     (IGFETs).
  
- 1     3.     The flip flop of claim 1, wherein said clocking portion further comprises:  
2             a second stack of transistors coupled to said second storage node to draw current  
3     from said second storage node when a second digital data value is being transferred to  
4     said state retention portion, said second digital data value being different from said first  
5     digital data value, said second stack of transistors including a third transistor having a  
6     gate terminal coupled to receive said clock signal and a fourth transistor having a gate  
7     terminal coupled to receive a delayed, inverted version of said clock signal.
  
- 1     4.     The flip flop of claim 3, wherein:  
2             said third and fourth transistors are N-type insulated gate field effect transistors  
3     (IGFETs).

1 5. The flip flop of claim 3, wherein:  
2 said gate terminal of said first transistor is connected to said gate terminal of  
3 said third transistor and said gate terminal of said second transistor is connected to said  
4 gate terminal of said fourth transistor.

1 6. The flip flop of claim 1, wherein said clocking portion comprises:  
2 a clock node to receive said clock signal; and  
3 an inversion device coupled between said clock node and said gate of said  
4 second transistor.

1 7. The flip flop of claim 6, wherein:  
2 said inversion device includes a conventional inverter.

1 8. The flip flop of claim 6, wherein:  
2 said inversion device includes a NOR gate having first and second input  
3 terminals and an output terminal, said first input terminal being connected to said clock  
4 node, said output terminal being connected to said gate terminal of said second  
5 transistor, and said second input being an enable input of said flip flop.

1 9. The flip flop of claim 1, wherein:  
2 said state retention portion includes a single latch.

1 10. The flip flop of claim 9, wherein:  
2 said single latch includes first and second inverters in a cross coupled  
3 configuration.

1 11. The flip flop of claim 10, wherein:  
2 said state retention portion includes a first pull up circuit connected between  
3 said first inverter and a power supply node and a second pull up circuit connected

4 between said second inverter and said power supply node, said first pull up circuit  
5 having a first pull up transistor and a second pull up transistor connected in parallel to  
6 provide two separate pull up paths for said first inverter.

1 12. The flip flop of claim 11, wherein:  
2 said first pull up transistor is larger than said second pull up transistor.

1 13. The flip flop of claim 3, further comprising:  
2 a next state generation portion, connected to said clocking portion, to receive  
3 said new bit of digital data from an external source before it is transferred to said state  
4 retention portion by said clocking portion.

1 14. The flip flop of claim 13, wherein:  
2 said next state generation portion includes at least one inversion device to invert  
3 a digital signal.

1 15. The flip flop of claim 14, wherein:  
2 said next state generation portion includes an input node and a first inversion  
3 device connected between said input node and an end of said first stack of transistors.

1 16. A flip flop comprising:  
2 a state retention portion to store a bit of digital data, said state retention portion  
3 including:  
4 first and second inverters arranged in a cross-coupled configuration;  
5 a first pull up circuit connected between said first inverter and a power  
6 supply node; and  
7 a second pull up circuit connected between said second inverter and said  
8 power supply node;

9                    wherein said first pull up circuit includes a first pull up transistor and a  
10                   second pull up transistor connected in parallel to provide two separate pull up  
11                   paths for said first inverter.

1    17.    The flip flop of claim 16, wherein:  
2                   said first pull up transistor is larger than said second pull up transistor.

1    18.    The flip flop of claim 16, comprising:  
2                   a next state generation portion to receive, at an input node thereof, a new bit of  
3                   digital data to be stored in said state retention portion; and  
4                   a clocking portion to transfer said new bit of digital data from said next state  
5                   generation portion to said state retention portion in response to a clock signal.

1    19.    The flip flop of claim 18, wherein said clocking portion comprises:  
2                   a first stack of transistors connected to an input of said first inverter, said first  
3                   stack of transistors including a first transistor having a gate terminal coupled to receive  
4                   said clock signal and a second transistor having a gate terminal coupled to receive a  
5                   delayed, inverted version of said clock signal.

1    20.    The flip flop of claim 19, wherein said clocking portion comprises:  
2                   a second stack of transistors connected to an input of said second inverter, said  
3                   second stack of transistors including a third transistor having a gate terminal coupled to  
4                   receive said clock signal and a fourth transistor having a gate terminal coupled to  
5                   receive a delayed, inverted version of said clock signal.

1    21.    The flip flop of claim 18, wherein:  
2                   said next state generation portion includes a first inversion device coupled  
3                   between said input node and an end of said first stack of transistors and a second

4 inversion device coupled between said end of said first stack of transistors and an end  
5 of said second stack of transistors.

1 22. A method comprising:  
2 providing a memory cell having first and second complementary storage nodes;  
3 providing a first transistor stack coupled to said first storage node of said  
4 memory cell, said first transistor stack having first and second transistors;  
5 providing a second transistor stack coupled to said second storage node of said  
6 memory cell, said second transistor stack having third and fourth transistors; and  
7 clocking a new data bit to said memory cell, wherein clocking includes:  
8 turning on said first and third transistors at a first instant in time; and  
9 turning off said second and fourth transistors a short period of time after  
10 said first instant in time.

1 23. The method of claim 22, wherein:  
2 clocking a new data bit to said memory cell includes:  
3 applying a clock signal to gate terminals of said first and third  
4 transistors; and  
5 applying a delayed, inverted version of said clock signal to gate  
6 terminals of said second and fourth transistors.

1 24. The method of claim 23, wherein:  
2 applying a delayed, inverted version of said clock signal to gate terminals of  
3 said second and fourth transistors includes applying said clock signal to an input of an  
4 inverter that has an output coupled to said gate terminals of said second and fourth  
5 transistors.

1    25.    The method of claim 22, wherein:  
2            applying a delayed, inverted version of said clock signal to gate terminals of  
3    said second and fourth transistors includes applying said clock signal to an input of a  
4    NOR gate that has an output coupled to said gate terminals of said second and fourth  
5    transistors.

1    26.    The method of claim 22, wherein:  
2            providing a memory cell includes providing first and second inverters in a cross  
3    coupled configuration, wherein said first complementary storage node includes an input  
4    to said first inverter and said second complementary storage node includes an input to  
5    said second inverter.

1    27.    A computing system comprising:  
2            a digital processing device having at least one flip flop including:  
3                    a state retention portion to store a bit of digital data, said state retention  
4                    portion having a first storage node and a second storage node, and  
5                    a clocking portion to transfer a new bit of digital data to said state  
6                    retention portion in response to a clock signal, said clocking portion including  
7                    a first stack of transistors coupled to said first storage node to draw current from  
8                    said first storage node when a first digital data value is being transferred to said  
9                    state retention portion, said first stack of transistors including a first transistor  
10                  having a gate terminal coupled to receive said clock signal and a second  
11                  transistor having a gate terminal coupled to receive a delayed, inverted version  
12                  of said clock signal; and  
13                  a flash memory coupled to said digital processing device.

1    28.    The computing system of claim 27, wherein:  
2            said clocking portion further comprises a second stack of transistors coupled to  
3    said second storage node to draw current from said second storage node when a second

4 digital data value is being transferred to said state retention portion, said second digital  
5 data value being different from said first digital data value, said second stack of  
6 transistors including a third transistor having a gate terminal coupled to receive said  
7 clock signal and a fourth transistor having a gate terminal coupled to receive a delayed,  
8 inverted version of said clock signal.

1 29. The computing system of claim 27, wherein:  
2 said clocking portion comprises a clock node to receive said clock signal and an  
3 inversion device coupled between said clock node and said gate of said second  
4 transistor.

1 30. The computing system of claim 27, wherein:  
2 said state retention portion includes a single latch.